New generation 2/3“, 9.5 Mpix CMOS imager combines charge-domain global shutter operation with exceptional high-speed capability

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Abstract. *Previously, when developing 2/3" imagers with native 4K resolution, it was necessary to decide whether they would support global shutter operation or high-speed operation, as both requirements could not be realized in a single imager. Furthermore, the sensitivity and dynamic range of even the best native 4K imagers did not reach the level that typical 2/3" HD imagers with their larger pixels have been offering for several years.*

Now, for the first time, a 2/3" CMOS imager based on a 65nm process offers 9.5 million pixels as required for UHDTV-1 resolution, with charge-domain global shutter operation and an output data rate of up to 114 Gb/s, enabling super slow-motion operation at full resolution.

This paper details the solutions and technologies used in this new generation of imagers and the resulting improved image parameters.

Keywords. CMOS Imager, Global shutter, UHDTV-1, HDR, CIS, 2/3-inch, high speed

Introduction

After the introduction of CCD cameras for broadcast applications in the late 1980s, the light sensitivity of the cameras improved realtively slowly. Over a long period of time, the light sensitivity only doubled every 6-10 years. It was only with the introduction of a completely new technology such as microlens technology for CCD sensors, the introduction of digital noise reduction in the first HD cameras, and more recently the transition from CCD sensor technology to CMOS sensor technology, that relatively large leaps in quality could be achieved from one camera generation to the next.

The use of three 2/3" sensors on a beam splitter and the B4 lens mount designed for it is now accepted as the optimal compromise for all typical applications in live production. Alternative solutions partly innate in the transition to higher resolution image formats such as smaller or larger sensor formats, one-sensor solutions, or even 4-sensor solutions could not establish themselves permanently. The reasons for this were explained in detail in various technical papers, including at the 2015 SMPTE conference [1].

The reduction in pixel size resulting from the constant imager size in combination with a larger number of pixels, as required in the transition from SD image formats to HD image formats and from HD image formats to UHDTV-1 operation, has a direct influence on the light sensitivity delivered by the sensors [2].

The increase in the number of pixels in UHDTV-1 operation compared to HD operation introduces challenges to the imaging technology. For example, the pixels, which are four times smaller for the same imager size, deliver four times less light sensitivity with the same imaging technology, and compensating for these losses alone would probably have taken over a decade in the past. In addition, the downsizing of the pixels poses further challenges in the area of dynamic range, maximum readout speed [3] and crosstalk between and within the pixels.

Until now, when developing 2/3" imagers with native UHDTV-1 resolution, it was necessary to decide whether they should support global shutter operation or high-speed operation, as both requirements could not be realized in one imager with the technologies available. Furthermore, the sensitivity and dynamic range of even the best UHDTV-1 imagers did not yet reach the level that typical 2/3" HD imagers with their larger pixels have been offering for several years.

A new 2/3" CMOS imager based on a 65nm process now offers, for the first time, 9.5 million pixels as required for UHDTV-1 resolution, with charge-domain global shutter operation and an output data rate of up to 114 Gb/s, enabling super slow-motion operation with 180 fps at full resolution.

Technology

Overview

Grass Valley has developed a global shutter CMOS imager with charge domain storage using the 65 nm CIS (CMOS Image Sensor) process [4]. The pixel size is 2.5 µm, with a total array size of 4224x2248, resulting in a resolution of 9.5 megapixels and an effective diagonal of 11 mm. The design focuses on high frame rate readout for broadcast applications. The high-level block diagram for the image sensor is shown in Figure 1.

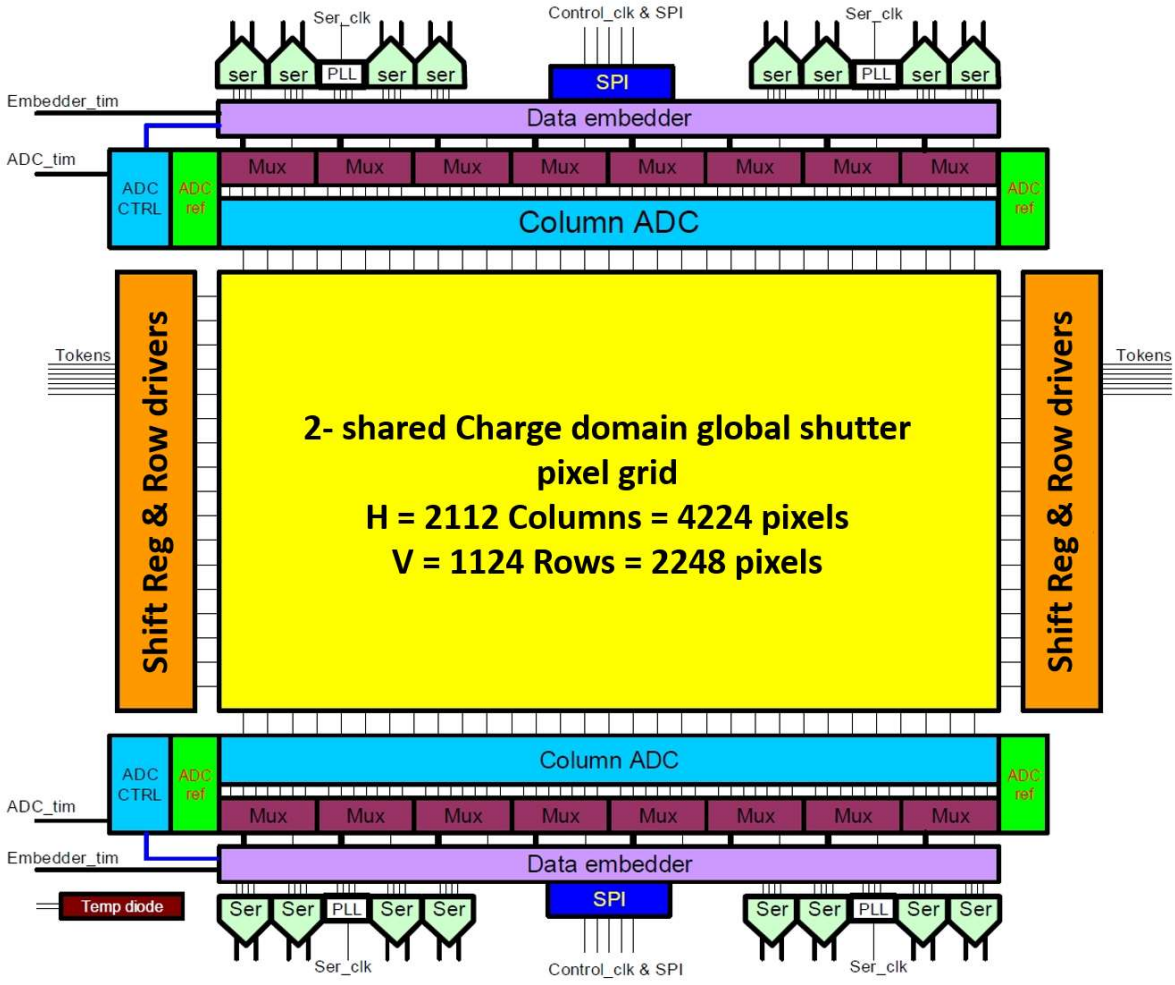

Figure 1 – Block diagram 2/3-inch image sensor with 9.5Mpix

The solution for column-based A/D conversion and multi-stage output multiplexing follows a similar concept to the previous generation imager presented at the 2020 SMPTE conference [3]. While the previous generation imager focused primarily on maximum readout speed, the new generation imager offers improved pixels and significantly better image performance, including nearly double sensitivity, significantly improved parasitic light sensitivity (PLS) and charge-domain global shutter operation even in UHDTV-1 high-speed operation.

Global shutter pixel

In recent years, there has been an increased demand for high-performance native 2/3" UHDTV-1 global shutter (GS) imagers that can capture images for broadcast without distortion of fast-moving objects, especially for high-speed sports productions.

Global shutter pixels can be divided into two types. One is the charge-domain type, where the charges generated in the photodiode are stored in a memory node (MN) [5,6]. The other is the voltage-domain type, where the charges generated in the photodiode are amplified in each pixel and then stored as a voltage in a capacitor. The voltage-domain type requires at least two switching transistors and capacitors when Correlation Double Sampling (CDS) is enabled, while the charge-domain type implements true CDS with only one additional storage node. In other words, the charge-domain type is more promising than the voltage-domain type, in terms of pixel scalability and low noise, and was chosen for the imager presented here (Fig. 2). In the practical application of the GS sensor, it is important to achieve a high signal-to-noise ratio. Since the charge-domain global shutter pixel has additional components such as the memory node compared to the rolling shutter pixel, suppression of the dark current generated in the memory node was one of the most important factors in the development of the charge-domain GS pixel.

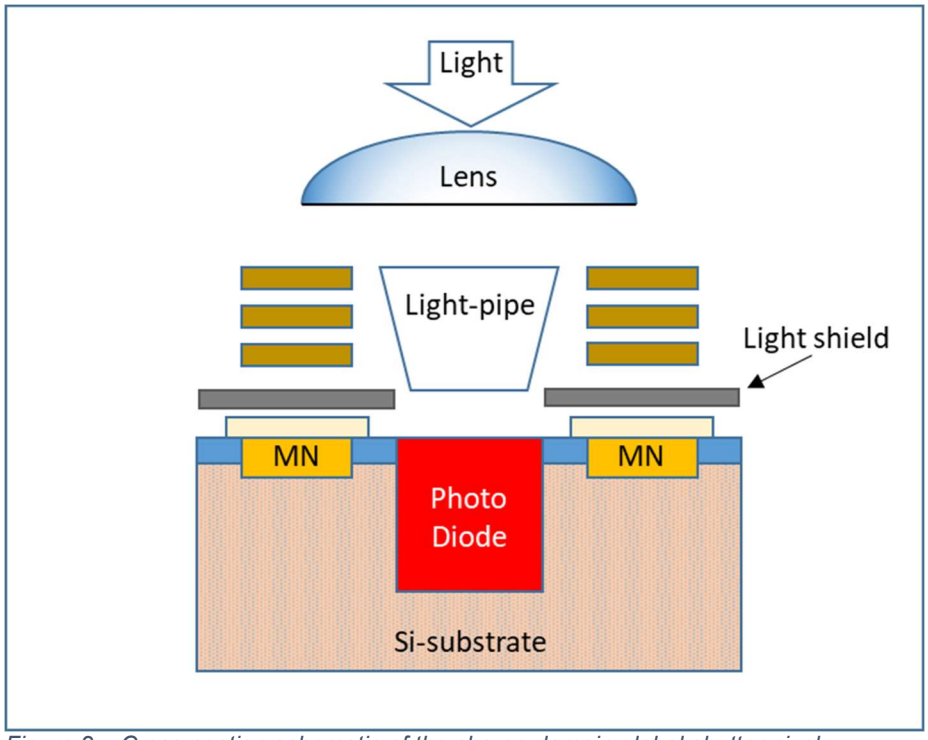

Figure 2 – Cross-section schematic of the charge domain global shutter pixel

PLS is generated by the light entering the MN and an increase in PLS leads to a deterioration in image quality. This is because the charges generated in the MN by the incident light are added to the charges stored in the MN from the PD after exposure. A pixel layout with optimised optical elements [5] significantly improves PLS performance compared to previous designs.

Pixel readout

The pixel used [5,6] is a selectless global shutter type with two diagonally divided charge regions. By bringing VDDC and reset (RST) to a high level, the pixel source follower for a certain row can be activated to drive the column.

This value is read as 'reset level'. The charge is now transported from the storage node (SN) to the floating diffusion (Cfd) by activating the transfer gate (TG_B), and the 'signal level' can be read. All these processes take place in series and each requires its own settling and transfer time, limiting the readout speed. For high frame rate readout, a second column is realized.

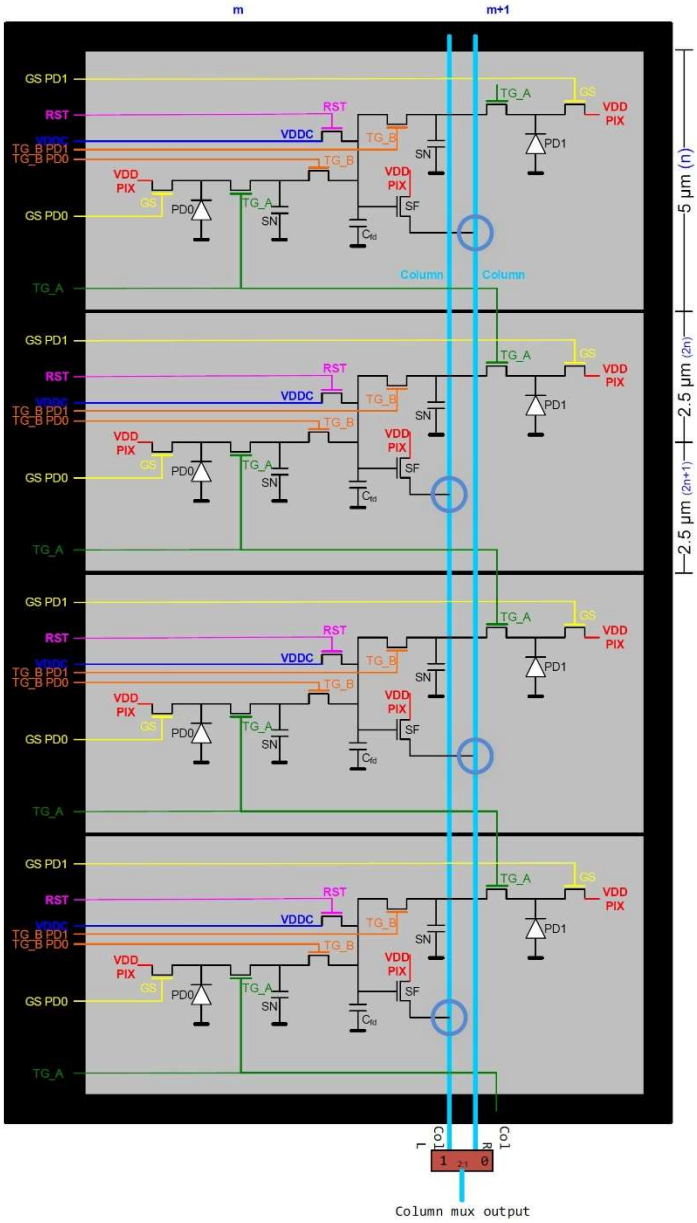

Figure 3 – Circuit diagram pixel with dual column

Figure 3 shows the pixel diagram with dual column. Two rows are operated in parallel to alternate the processes of column sampling, pixel reset and charge transfer SN to Cfd. In this way, the throughput of reset and signal levels from the pixel array is maximised.

Figure 4 shows a timing diagram for a selectless pixel with a single-column and a dual-column readout comparison.

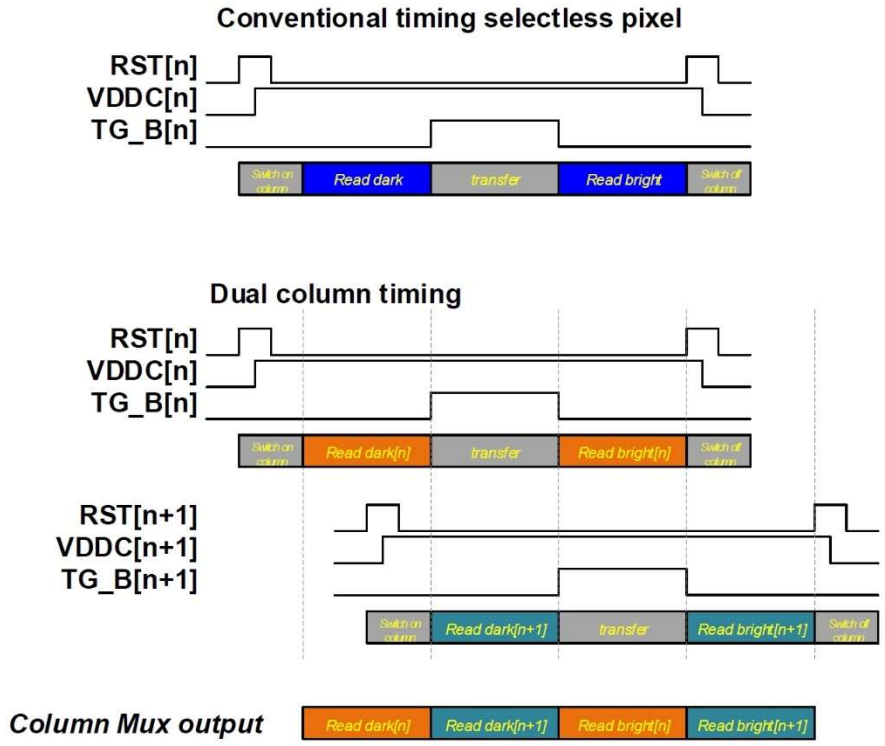

Figure 4 - Timing diagram single- vs dual-columns

The pixel values are sampled on the digital sub-ranging, charge-based column analog-to-digital Converter (ADC) built on the concept of [7]. The ADC converts the high input range signal into a 16bit output. In this way, the pixel low-noise values and the high full-well values are preserved and the full dynamic range is maintained.

The digital output data of the 2112 column ADCs are serialized by a hybrid output multiplexer [8]. A data embedder processes the ADC data.

A cyclic redundancy check (CRC) inserter is introduced to monitor the integrity of the serializer links between the imager and the receiving field-programmable gate array (FPGA). The data embedder also implements training-pattern insertion, scrambling, daisy chaining and takes care of the correct mapping of the data with a barrel shifter to the serializer in the case of 16/14 bit output modes.

After processing, the data is delivered to the serializer blocks [9]. The serializer has programmable serialization widths of 28 or 32 bit.

The output is compatible with the JESD8-13 standard which defines the input, output, and termination specifications for differential signaling in the scalable low-voltage signaling for 400 mV (SLVS-400) environment and runs at up to 7.1 Gb/s per channel. The imager has 16 such lanes resulting in a total output data rate of up to 114 Gb/s.

Results

Figure 5 shows an example of an output image of the imager described here, demonstrating global shutter operation of the imager.

The imager was operated with 60 fps and a short exposure time of 1 millisecond. A symmetrical motion blur can be seen on the fan blades, as would be expected in global shutter operation, whereas in rolling shutter operation a completely distorted shape of the fan blades would be expected.

Figure 5 - Sample UHD image at 60 fps with integration time of 1ms

The outputs of the serialiser run at 7.1 Gbit/s, in a custom ceramic package. The measurement results are shown in figures 6 and 7.

Figure 6 shows the eye diagram of the SLVS outputs at 7.1 Gb/s.

Eye diagrams are the oldest and most widely used conformance methodology for high-speed serial links. The appearance of the eye diagram allows a visual assessment of the performance of a channel and a quick evaluation of the key parameters of the signal. The more open an eye is, the less likely it is that a bit in the data stream has been received in error. The eye diagram of the SLVS output signal in Figure 6 is wide open, which suggests stable and reliable transmission.

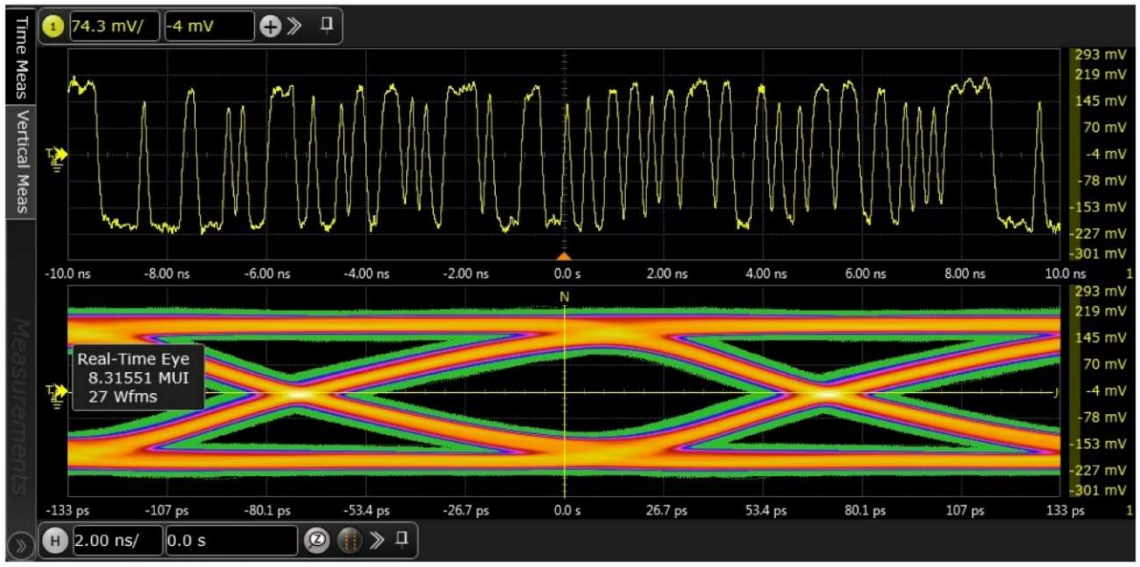

Figure 6 - Eye diagram SLVS output at 7.1 Gb/s

Figure 7 shows the bit error ratio (BER) bathtub and total jitter histogram of the LVDS outputs.

The bathtub curve provides good insight into the BER performance of a link under test. The bathtub curve is useful because it can provide a lot of insight into the behavior of a system. Apart from estimating BER, it also provides an indication for the amount of margin that is in the system. The BER bathtub diagram and the total jitter histogram in Figure 7 show a good BER and low jitter with sufficient margins for stable and reliable operation.

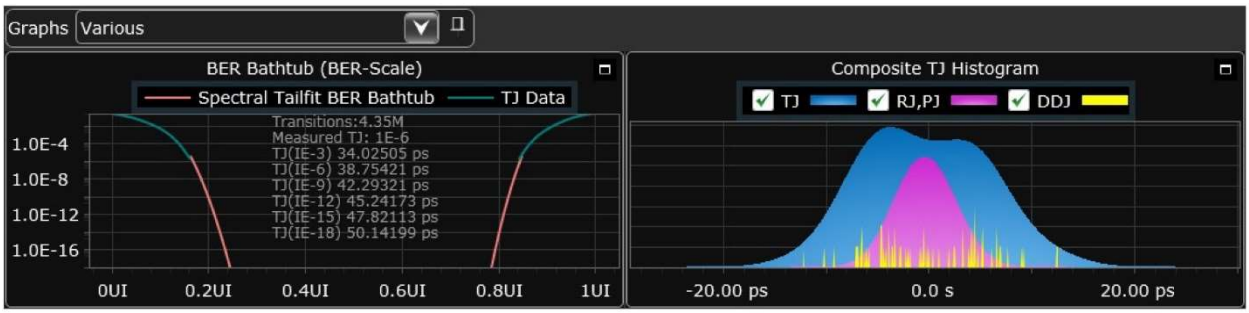

Figure 7 - Serializer BER bathtub and total jitter histogram

The performance measurements show a system noise of 1.9e-read noise at 7ke-linear fullwell. The imager shows no lag and the 1/PLS is measured at >80dB in green. A list of detailed parameters is shown in figure 8.

Parameter	Unit	Value	Note
Resolution	#	4224 (H) x 2248 (V)	9.5 Mpix
Pixel size	µm	2.5	
Shutter type		Global	Charge domain storage
Noise	e-	1.9	
Full well [e-]	e-	7000	
PLS	dB	-80	Typ @ F11
MTF @ 800 TVL	%	40	
Framerate after CDS	Fps	240	
ADC type		Column wise	Charge based digital multi-slope
ADC count	#	2112	Sum of north and south
ADC noise	µV	120	
ADC resolution	#	14 to 16 bit	240 to 60 Hz framerate
ADC conversion time	ns	<450	
Output interface		SLVS	
# of channels	#	16	
Data rate per channel	Gbps	7.2	
Package		Custom ceramic 215 pin PGA	
Technology node		65 nm, 1P4M	
Die area	mm²	210	
Control		SPI	
Power	W	1.9 to 3.5	60 to 240 Hz output framerate

Figure 8 – Parameter list

Conclusion

There is a need for native 2/3" UHDTV-1 imagers that support global shutter in combination with high-speed operation, especially for demanding live sports productions. However, until now there have only been 2/3" imagers with UHDTV-1 resolution that support either global shutter operation or high-speed operation, but not both requirements together.

Furthermore, the sensitivity and dynamic range of even the best native 4K imagers were not yet at the level that typical 2/3" HD imagers, with their larger pixels, have been achieving for several years.

A new generation of 2/3" CMOS imagers based on a 65nm CIS process now offers, for the first time, 9.5 million charge-domain global shutter pixels with significantly improved light sensitivity, an extended dynamic range and an output data rate enabling super slow motion operation with 180 fps at full UHDTV-1 resolution.

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